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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,525	09/29/2003	John Bruno	00100.03.0034	6091

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,525	BRUNO ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received May 16, 2006 for application number 10/675525 originally filed September 29, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-33 wherein claims 1-11, 14 and 20-33 have been cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, 13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (U.S. Patent Publication No. 2004/0088593) (hereinafter referred to as Park) in view of Meynard (U.S. Patent Publication No. 2003/0229816 A1) (hereinafter referred to as Meynard) and Mahalingaiah et al. (U.S. Patent No. 5,490,059) (hereinafter referred to as Mahalingaiah).

As to claim 12, Park discloses a clock control system for generating a clock signal having an operating frequency set to a first operating frequency corresponding to a threshold temperature, comprising: a thermal sensor (5) operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die (paragraph 20); a thermal sensor control circuit (10), operatively coupled to the thermal sensor (as shown in figure 1), and operative to produce temperature data in response to the temperature signal

(produces a "higher temperature value") and to provide a control signal in response to the temperature data (paragraph 21, lines 9-16); a clock generator circuit (3) operative to produce the clock signal (paragraph 20); and a dynamic overclock frequency control data generator (16), operatively coupled to the thermal sensor control circuit and the clock generator circuit (as shown in figure 1), and operative to provide dynamic overclock frequency control signal to the clock generator circuit (sends a control signal to the operation frequency controller 3) in response to the control signal and the received temperature data (temperature data received at linear signal generator 14; paragraph 22, lines 1-6) to cause the clock generator circuit to increase the operating frequency of the clock signal when the detected junction temperature is less than a threshold temperature (Park discloses the operation frequency controller 3 receiving a control signal from driving circuit 18 that increases the frequency of the CPU 1 dependent on the temperature detected; paragraphs 21 and 35).

Park does not disclose a method that can overclock a processor where the operating frequency is set above the nominal frequency of the processor if the junction temperature is below a maximum rated temperature.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56). Meynard has the additional feature of allowing the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

It would have been obvious to one of ordinary skill of the art, having the teachings of Park and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Park to use the overclocking capabilities as taught by Meynard. One of ordinary

skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would give the added benefit of allowing the activity of the system to determine saturation and stalls in the system (as taught by Meynard above).

Neither Park nor Meynard teaches the dynamic overclock frequency control data generator sending providing dynamic overclock frequency control data to the clock generator circuit.

Mahalingaiah teaches a clock speed optimizing mechanism wherein a control unit (134) sends control data (122) to a frequency synthesizer that clocks a CPU (102) (column 3, lines 33-40). Mahalingaiah also has the additional feature of controlling the frequency of the system clock (column 2, lines 2-7).

It would have been obvious to one of ordinary skill of the art, having the teachings of Park, Meynard and Mahalingaiah before him at the time the invention was made, to modify the dynamic overclock frequency control data generator disclosed by Park to determine and deliver clock control data as taught by Mahalingaiah. One of ordinary skill in the art would be motivated to make use of determining and delivering clock control data in view of the teachings of Mahalingaiah, as doing so would give the added benefit of controlling the frequency of the system clock (as taught by Mahalingaiah above).

As to claim 13, Park together with Meynard and Mahalingaiah taught the clock control system according to claim 12, as described above. Mahalingaiah further teaches wherein the dynamic clock frequency control data generator (16) is operative, in response to the control signal, to provide hysteresis based frequency control (column 3, lines 6-15) to increase the

operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold (column 3, line50 thru column 5, line 42).

Meynard further teaches decreasing the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold. (paragraphs 29 and 53-56).

As to claim 15, Park together with Meynard and Mahalingaiah taught the clock control system according to claim 12, as described above. Park further teaches wherein the thermal sensor control circuit is operative to produce the control signal in response to a comparison between the temperature data and the threshold temperature data (paragraph 21, lines 9-16).

As to claim 16, Park together with Meynard and Mahalingaiah taught the clock control system according to claim 12, as described above. Mahalingaiah further teaches wherein the dynamic overclock frequency control data generator is operative to reduce the frequency of the clock signal to at least the portion of the circuit on the die in response to the control signal and if the first junction temperature is above a junction temperature threshold (column 3, lines 33-40).

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Culbert et al. (U.S. Patent No. 6,820,209 B1) (hereinafter referred to as Culbert) in view of Meynard (U.S. Patent Publication No. 2003/0229816 A1) and Park (U.S. Patent Publication No. 2004/0088593).

As to claim 17, Culbert discloses in a system comprising a host processor (102) and a graphics co-processor (Culbert discloses a graphics controller 116 that "provides processing of display commands" and therefore a co-processor; column 4, lines 30-34), a method for

generating a clock signal (via clock controller 218 within 116) for the graphic co-processor (column 6, line 56 thru column 7, line 41).

Culbert does not disclose the method wherein the clock signal has an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56). Meynard further discloses that the overclocking is carried out dependent upon keeping the processor to "comply with the specifications of the product manufacturer" which is inclusive of temperature and therefore maximum rated temperature (paragraphs 38, 46 and 62). Meynard has the additional benefit of allowing the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

It would have been obvious to one of ordinary skill of the art, having the teachings of Culbert and Meynard before him at the time the invention was made, to modify the clock control methods disclosed by Culbert to use the overclocking capabilities based upon the maximum rated temperature as taught by Meynard such that the host processor overclocks the graphics co-processor of Culbert based upon the maximum rated temperature. One of ordinary skill in the art would be motivated to make use of overclocking capabilities based upon the maximum rated temperature in view of the teachings of Meynard, as doing so would give the added benefit of allowing the activity of the system to determine saturation and stalls in the system (as taught by Meynard above).

Neither Culbert nor Meynard teach: detecting, by a thermal sensor coupled to the graphics co-processor, a junction temperature corresponding to at least a portion of a circuit on a die constituting at least a portion of the graphics co-processor, thereby providing a temperature signal; providing, by a thermal sensor control circuit coupled to the thermal sensor, a control signal and temperature data in response to the temperature signal; and causing, by the host processor coupled to the thermal sensor control circuit and in response to the control signal and the temperature data, an in crease in the operating frequency of the clock signal when the detected junction temperature is below a threshold temperature.

Park teaches an overheating protection system and method of a processor (31) the method comprising: detecting, by a thermal sensor (35) coupled to the processor (31) (as shown in figure 2), a junction temperature corresponding to at least a portion of a circuit on a die constituting at least a portion of the processor, thereby providing a temperature signal (paragraph 28 and paragraph 30, line 1-5); providing, by a thermal sensor control circuit (40) coupled to the thermal sensor (as shown in figure 2), a control signal (signal sent to 54) and temperature data (produces a "higher temperature value") in response to the temperature signal (paragraph 30); and causing, by the host processor (micom 54; paragraph 13) coupled to the thermal sensor control circuit (as shown in figure 2) and in response to the control signal (sent to 54) and the temperature data (responsible for producing the control signal sent to 54), an increase in the operating frequency of the clock signal (Park discloses an operation frequency controller 46 receiving a control signal from micom 54 and sending a control signal from driving circuit 18 within frequency controller 46 that increases the frequency of the processor 31 dependent on the temperature detected;

paragraphs32, 33 and 35). Park also has the additional feature of monitoring the heat sensed within a power supply (paragraph 11).

It would have been obvious to one of ordinary skill of the art, having the teachings of Culbert, Meynard and Park before him at the time the invention was made, to modify the clock control methods disclosed by Culbert to use the clock control methods as taught by Park such that the host processor controls the clock frequency of the graphics co-processor of Culbert based upon the temperature ranges and thresholds via thermal sensors and a thermal sensor control unit. One of ordinary skill in the art would be motivated to make use of clock altering capabilities based upon the temperatures sensed in a processor in view of the teachings of Park, as doing so would give the added benefit of the heat sensed within a power supply (as taught by Park above).

As to claim 18, Culbert together with Meynard and Park taught the clock control method for a graphics co-processor according to claim 17, as described above. Culbert further teaches changing, by the host processor in response to the control signal (SYS_CMD), altering the graphics co-processor clock (column 7, lines 17-41).

Meynard further teaches the method including decreasing the operating frequency of the clock signal below the nominal operating frequency when the detected junction temperature is above the maximum rated junction temperature (Meynard teaches forcing the frequency back to a first in response to the processor temperature; paragraph 29).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Culbert et al. (U.S. Patent No. 6,820,209 B1), Meynard (U.S. Patent Publication No. 2003/0229816 A1) and

Park (U.S. Patent Publication No. 2004/0088593) as applied to claims 17 and 18 above, and further in view of Borkar et al. (U.S. Patent No. 6,484,265 B2) (hereinafter referred to as Borkar).

As to claim 19, neither Culbert, Meynard nor Park discloses the method further including providing hysteresis based frequency control.

Borkar teaches frequency controlling method for a processor based upon the temperature sensed in the processor and providing hysteresis based frequency control (column 4, lines 13-43). Borkar has the added feature of controlling voltage supplied to the processor in addition to the clock signal (column 1, line 66 thru column 2, line 3).

It would have been obvious to one of ordinary skill of the art, having the teachings of Culbert, Meynard, Park and Borkar before him at the time the invention was made, to modify the clock control methods disclosed by Culbert to use the clock control methods as taught by Borkar therefore providing hysteresis based frequency control. One of ordinary skill in the art would be motivated to make use of hysteresis based frequency control upon the temperatures sensed in a processor in view of the teachings of Borkar, as doing so would give the added benefit of controlling voltage supplied to the processor in addition to the clock signal (as taught by Borkar above).

Response to Arguments

Applicant's arguments with respect to claim 12-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or (571) 272-1000.

James Sugent
Patent Examiner, Art Unit 2116
June 21, 2006

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